

APPLICATION FOR LETTERS PATENT

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Transistor Structures, Methods of Forming Transistor Structures, and Methods of Forming Insulative Material Against Conductive Structures

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ATTORNEY'S DOCKET NO. MI22-1332

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1 Transistor Structures, Methods of Forming Transistor Structures, and
2 Methods of Forming Insulative Material Against Conductive Structures

3 **TECHNICAL FIELD**

4 The invention pertains to methods of forming insulative materials
5 against conductive structures, and in particular aspects pertains to
6 methods of forming transistor structures. Also, the invention pertains to
7 transistor structures.

8
9 **BACKGROUND OF THE INVENTION**

10 A frequently used procedure of semiconductor fabrication is
11 formation of a so-called "self-aligned contact" (SAC) opening. An
12 exemplary use of a SAC opening is to expose a node between a pair of
13 wordlines, and can be conducted as follows. First, a pair of adjacent
14 wordlines are formed over a substrate, and then insulative sidewall
15 spacers are formed along conductive portions of the lines. The
16 wordlines typically comprise conductive portions capped by insulative
17 material. Suitable insulative material for capping the wordlines is silicon
18 nitride. A thick insulative layer (typically borophosphosilicate glass
19 (BPSG)) is formed over the wordlines and insulative sidewall spacers.
20 The insulative sidewall spacers are formed of a material different than
21 the thick insulative layer, with a suitable material being silicon nitride.

22 An opening is etched through the thick insulative layer and to an
23 electrical node between the wordlines. If the thick insulative layer

1 comprises BPSG and the sidewall spacers comprise silicon nitride, the
2 etch utilizes conditions which are selective for the BPSG relative to the
3 silicon nitride. The insulative spacers are exposed during formation of
4 the opening, but are etched more slowly than the BPSG, and preferably
5 are not entirely removed by the etch of the BPSG. The opening is
6 intended to be formed to have a periphery "aligned" with the spacers,
7 and the formation of the opening is referred to as a "self-aligned
8 contact" etch.

9 It is desired that the spacers not be entirely removed during
10 formation of the opening so that the spacers can protect the conductive
11 material of the wordlines from being exposed when the opening is
12 formed. If the conductive material of the wordlines becomes exposed in
13 the openings, device failure will likely result. A problem with current
14 semiconductor fabrication processes is that silicon nitride insulative
15 spacers are occasionally over-etched during formation of contact openings
16 in BPSG, leading to exposure of wordline conductive material, and to
17 device failure.

18 A possible method for overcoming the above-discussed problem is
19 described in U.S. Pat. No. 5,700,349, which suggests utilizing $\text{Si}_x\text{O}_y\text{N}_z$ or
20 Al_xO_y based materials to protect conductive portions of a wordline during
21 a SAC method. The utilization of $\text{Si}_x\text{O}_y\text{N}_z$ and Al_xO_y as protective
22 materials relative to the conductive material of a wordline during a SAC
23 method shows promise, in that $\text{Si}_x\text{O}_y\text{N}_z$ and Al_xO_y appear to be more

1 the electrically conductive material of the sidewall of the transistor gate.
2 The electrically insulative material comprises at least one of $\text{Si}_x\text{O}_y\text{N}_z$ and
3 Al_pO_q , wherein p, q, x, y and z are greater than 0 and less than 10.
4 A layer consisting of silicon dioxide is over the transistor gate,
5 electrically insulative material and substrate. A layer of BPSG is over
6 the layer consisting of silicon dioxide.

8 BRIEF DESCRIPTION OF THE DRAWINGS

9 Preferred embodiments of the invention are described below with
10 reference to the following accompanying drawings.

11 Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a
12 portion of a semiconductor wafer at an initial processing step of a
13 method of the present invention.

14 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a
15 processing step subsequent to that of Fig. 1.

16 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a
17 processing step subsequent to that of Fig. 2.

18 Fig. 4 is a view of the Fig. 1 wafer fragment shown at a
19 processing step subsequent to that of Fig. 3.

20 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a
21 processing step subsequent to that of Fig. 4.
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1 Fig. 6 is a view of the Fig. 1 wafer fragment shown at a
2 processing step subsequent to that of Fig. 1 in accordance with a second
3 embodiment of the present invention.

4 Fig. 7 is a view of the Fig. 6 wafer fragment shown at a
5 processing step subsequent to that of Fig. 6.

6 Fig. 8 is a view of the Fig. 6 wafer fragment shown at a
7 processing step subsequent to that of Fig. 7.

8 Fig. 9 is a view of the Fig. 6 wafer fragment shown at a
9 processing step subsequent to that of Fig. 8.

10 11 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

12 This disclosure of the invention is submitted in furtherance of the
13 constitutional purposes of the U.S. Patent Laws "to promote the progress
14 of science and useful arts" (Article 1, Section 8).

15 In one aspect, the invention is a recognition that deposited
16 antireflective coating (DARC) materials (which are typically $\text{Si}_x\text{O}_y\text{N}_z$,
17 wherein x, y and z are greater than 0 and less than 10) can be utilized
18 to protect conductive materials of wordlines during an etch of BPSG
19 (such as, for example, during a SAC etch).

20 The invention also encompasses a recognition that if $\text{Si}_x\text{O}_y\text{N}_z$ is
21 utilized to protect a conductive material during an etch, the $\text{Si}_x\text{O}_y\text{N}_z$ is
22 preferably electrically insulative. The $\text{Si}_x\text{O}_y\text{N}_z$ can then function to
23

prevent shorting between the protected conductive material and other conductive materials proximate the protected conductive material.

Further, the invention encompasses a recognition that $\text{Si}_x\text{O}_y\text{N}_z$ can have different characteristics if dopant is provided therein relative to if the material is undoped. Specifically, if dopant permeates within $\text{Si}_x\text{O}_y\text{N}_z$, the material can develop conductive characteristics which will destroy its ability to function as an electrically insulative protective layer. Dopant can migrate from a doped oxide (such as, for example, BPSG) provided against $\text{Si}_x\text{O}_y\text{N}_z$, and accordingly the invention encompasses provision of a dopant barrier layer between $\text{Si}_x\text{O}_y\text{N}_z$ and a doped oxide provided proximate the $\text{Si}_x\text{O}_y\text{N}_z$.

Dopant migration problems may also occur relative to materials comprising Al_pO_q (wherein p and q are greater than 0 and less than 10), and accordingly the invention also comprises provision of a dopant barrier layer between materials comprising Al_pO_q and doped oxide (such as, for example, BPSG).

A first embodiment method of the present invention is described with reference to Figs. 1-5. Referring initially to Fig. 1, a semiconductor wafer fragment 10 comprises a semiconductive material substrate 12 having wordlines 14, 16, 18 and 20 formed thereover. Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and

